REMARKS

OBJECTIONS TO THE SPECIFICATION:

The Examiner objects to the Abstract for the use of phrases which may be implied. Applicants have amended the abstract to remove the objectionable language. Accordingly. Applicants respectfully request reconsideration and withdrawal of this objections.

REJECTION UNDER 35 USC 102(e):

Claims 1-8 are rejected under 35 USC 102(e) as being anticipated by U.S. Patent Application No. 2004/0109348 filed by Ooishi ("*Ooishi*"). Applicants respectfully traverse this rejection. Applicants have amended independent Claims 1 and 5 to clarify the precise manner in digit currents are provided to a plurality of magnetic memory cells. Specifically, amended Claim 1 now recites "providing a plurality of predetermined digit currents I_D in parallel in the plurality of digit lines at a predetermined digit line voltage V_D for the plurality of magnetic memory cells at substantially the same time as the bit line current I_B the plurality of digit currents and the bit line current allowing the plurality of magnetic memory cells to be written to a plurality of states in parallel, wherein the total power supplied to the plurality of magnetic memory cells during writing is $I_BV_B + NI_DV_D$, where N is the number of digit lines." Amended Claim 5 similarly recites "at least one write circuit configured to provide a predetermined bit line current I_B in the bit line at a predetermined bit line voltage V_B and to provide a plurality of predetermined digit currents I_D in parallel in the plurality of digit lines at a predetermined digit line voltage V_D in parallel at substantially the same time as the bit line current I_B, the plurality of digit currents and the bit line current allowing the plurality of magnetic memory cells to be written to a plurality of states in parallel, wherein the total power supplied to the plurality of magnetic memory cells during writing is $I_BV_B + NI_DV_D$, where N is the number of digit lines."

Ooishi fails to describe, either expressly or inherently, the quoted limitations of Claims 1 and 5. *Ooishi* provides no express teaching regarding the total power provided to the memory cells described in *Ooishi* by the digit and bit lines. Nor is a

disclosure of the quoted limitations inherent in *Ooishi* for at least two reasons. First, the timing diagrams in *Ooishi*, such as those illustrated in Fig. 16, do not indicate that the separate constant current circuits corresponding to the digit lines are simultaneously active. Second, even if the constant current circuits were all active simultaneously, the variation in the voltage of the output node of constant current sources (VD in Fig. 16) to prevent excessive voltage buildup (charging current) would prevent the write current from being supplied in the manner recited in Claims 1 and 5. Thus, *Ooishi* does not describe, expressly or inherently, all of the elements of independent Claims 1 and 5. All other pending claims depend on Claims 1 and 5 and are also allowable for at least the reasons presented above. For at least these reasons, then, Applicants respectfully request reconsideration and allowance of all pending claims.

CONCLUSION

In view of the foregoing amendments and/or remarks, Applicants respectfully submit that the pending claims are now in condition for allowance and requests reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1055.

Respectfully submitted,

Date: 3/20/06

By: _____
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